1. (currently amended) In a digital display device including a clock recovery system for recovering a system time clock reference from a video bit-stream generated at an encoder to produce a decoder system clock frequency, and a decoding system for decoding and decompressing the video bitstream at a frame rate, an adaptive clocking mechanism for said decoding system comprising: means for extracting from said video bit stream attributes of a video format transmitted via said bitstream; selecting means, cooperatively linked with said decoding system, for selecting a modifier from a group of modifiers based on video format attributes derived from said video bit-stream; and modifying means, cooperatively linked with said selecting means and said decoding system, for modifying a synchronization timing parameter of said decoding system with said selected modifier prior to decoding said video bit-stream, wherein the group of modifiers includes the ratios 1/1, 1000/1001, and 1001/1000.

2. (original) The adaptive clocking mechanism of claim 1, wherein said modifying means comprises means for applying said selected modifier to a system clock frequency provided by said clock recovery system.

3. (original) The adaptive clocking mechanism of claim 1, wherein said selecting means comprises a software routine, said group of modifiers consists of ratios of frame rates selectable at said encoder, said synchronization timing parameter includes a frame rate applied by said decoder, and wherein said modifying means modifies said decoder frame rate by applying said selected modifier to said system clock frequency.

4. (original) The adaptive clocking mechanism of claim 3, wherein said modifying means comprises phase-locked loop circuitry.

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5. (original) The adaptive clocking mechanism of claim 1, wherein said synchronization timing parameter is a frame rate applied by said decoder, and said modifying means modifies said frame rate by applying said modifier selected by said selecting means to said system time clock.

6. (original) The adaptive clocking mechanism of claim 1, wherein said selecting means comprises a software routine, said group of modifiers consists of ratios of frame rates selectable at said encoder, said synchronization timing parameter includes a frame rate applied by said decoder, and wherein said modifying means modifies said decoder frame rate by applying said selected modifier to said system time clock.

7. (original) The adaptive clocking mechanism of claim 6, wherein said clock recovery system is modified to include a multiplier having as a first input a system time clock signal and as a second input signal a selected one of said frame-rate ratios, and an output, representing a product of said first and said second inputs, which is provided as an input to a differentiator/subtractor having as a second input a clock reference signal derived from said video bitstream, wherein an output of said clock recovery system is modified in proportion to said selected one of said frame-rate ratios inputted two said multiplier.

8. (currently amended) A method for providing synchronization of a video decoder for an input video bitstream encoded in respect to a given video format, where said given video format may be characterized by a preferred frame rate or by an alternate frame rate, said method comprising the steps of: operating on said input video bitstream to derive therefrom one or more attributes of said given video format, said attributes having a known relationship to said given video format; detecting from said derived attributes an identify of

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said given video format and an indication of whether said encoded input video bitstream is characterized by said preferred frame rate or said alternate frame rate; where said encoded input video bitstream is characterized by said alternate frame rate, selecting a modifier for application to a synchronization timing function of said decoder, said modifier being related to a differential between said preferred frame rate and said alternate frame rate; and applying said modifier to said decoder synchronization function, wherein the modifier is a preferred to alternate frame rate ratio of 1000/1001.

9. (original) The video decoder synchronization method of claim 8 wherein said attributes of said given video format include an encoded pixel rate, line rate and frame rate for said input video bitstream.

10. (original) The video decoder synchronization method of claim 9 wherein each said given video format is characterized by a unique combination of the said encoded pixel rate, line rate and frame rate.

11. (original) The video decoder synchronization method of claim 8 wherein said synchronization function is a system time clock for said decoder and said step of applying said modifier operates to effect an adjustment in a rate of said system time clock.

12. (original) The video decoder synchronization method of claim 11 wherein said modifier is proportional to a ratio of values of said preferred frame rate and of said alternate frame rate.

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13. (original) The video decoder synchronization method of claim 8 wherein said synchronization function is

a clock recovery function of said decoder and said step of applying said modifier operates to effect an

adjustment in an output rate of said clock recovery function.

14. (original) The video decoder synchronization method of claim 13 wherein said application of said modifier

to said clock recovery function includes a multiplication function integral to the said clock recovery function

having as a multiplier input said selected modifier.

15. (original) The video decoder synchronization method of claim 14 wherein said modifier is proportional

to a ratio of values of said preferred frame rate and of said alternate frame rate.

16. (original) The video decoder synchronization method of claim 8 wherein values of said preferred frame

rate and of said alternate frame rate are related according to a known ratio.

17 (canceled).

18. (currently amended) ~~The video decoder synchronization method of claim 11 wherein said known~~ A method

for providing synchronization of a video decoder for an input video bitstream encoded in respect to a given

video format, where said given video format may be characterized by a preferred frame rate or by an alternate

frame rate, said method comprising the steps of: operating on said input video bitstream to derive therefrom

one or more attributes of said given video format, said attributes having a known relationship to said given

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video format; detecting from said derived attributes an identify of said given video format and an indication of whether said encoded input video bitstream is characterized by said preferred frame rate or said alternate frame rate; where said encoded input video bitstream is characterized by said alternate frame rate, selecting a modifier for application to a synchronization timing function of said decoder, said modifier being related to a differential between said preferred frame rate and said alternate frame rate; and applying said modifier to said decoder synchronization function, wherein the modifier is a preferred to alternate frame rate ratio [[is]] of 1001/1000.

19. (original) The video decoder synchronization method of claim 11, wherein said modifier is proportional to said known ratio.

20. (currently amended) A frame rate modifier for a digital display device comprising: means for selecting a modifier based on format information values from a video bitstream received by the digital display device, said format information values including a system time clock reference value; and, means for modifying at least one of said format information values, by applying said selected modifier, in order to adjust a frame rate at which input information is operated on by a decoding device associated with said digital display device, wherein the modifier is selected from a group consisting of ratios of frame rates including the ratios 1/1, 1000/1001, and 1001/1000.

21. (original) The frame rate modifier of claim 20 wherein a system clock frequency is produced from said system time clock reference value, wherein said means for selecting comprises means for selecting said

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modifier from a group consisting of ratios of frame rates selectable at an encoder transmitting said bitstream, and said means for modifying comprises means for applying said modifier to said system clock frequency.

22. (canceled).

23. (original) The frame rate modifier of claim 21, wherein said means for modifying is further defined by phase-locked loop circuitry.

24. (original) The frame rate modifier of claim 20, wherein said means for modifying comprises means for modifying said system time clock.

25. (original) The frame rate modifier of claim 24, wherein said means for modifying comprises a multiplier.

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